UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,777	11/19/2001	Craig Nemecek	CYPR-CD01208M	2046

7590 04/11/2006	EXAMINER
WAGNER, MURABITO & HAO LLP	SHARON, AYAL I

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/989,777	NEMECEK, CRAIG
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2006*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-28 of U.S. Application 09/989,777 are currently pending. The application was originally filed on filed on 11/19/2001.

2. Claims 1 and 7 have been amended.

3. Examiner has accepted Applicant's amendment to the specification and amended Figure 7.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/10/06 has been entered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. The prior art used for these rejections is as follows:

7. Profit. Jr., U.S. Patent 5,911,059. (Henceforth referred to as "**Profit**").

8. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

9. **Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Profit.**

10. In regards to Claim 1,

> 1. A method for performing a sleep operation in a system that includes a device under test and an emulator device, said method comprising:
>
> a) executing instructions on said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

> b) emulating the functions of said device under test by operating said emulator device in lock-step fashion with said device under test; and

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> c) performing a sleep operation, comprising:

c1) upon receiving a first signal that indicates that a sleep function is to be performed, initiating said sleep function at said device under test;

c2) turning off one or more clock of said device under test; and

c3) discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

11. In regards to Claim 2,

2. The method of Claim 1 wherein said clock comprises an internal CPU clock.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

12. In regards to Claim 3,

3. The method of Claim 2 wherein said first signal is generated by said device under test and is transmitted internally to a register that indicates that a sleep function is to be performed.

Examiner finds that the memory (Fig.7, Item 206) corresponds to claimed register. See col.12, lines 4-11 for more details.

13. In regards to Claim 4,

4. The method of Claim 1 further comprising:

> when said sleep function has been completed by said device under test, turning on said clock and sending a second signal from said device under test to said emulator device;
>
> receiving said second signal at said emulator device;
>
> determining the number of clock signals received at said emulator device since said second signal was received; and
>
> resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

14. In regards to Claim 5,

> 5. The method of Claim 4 wherein said device under test further comprises a microcontroller and wherein said first signal comprises a first bit, said first bit received at a register of said microcontroller to indicate that a sleep function is to be performed.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

15. In regards to Claim 6,

> 6. The method of Claim 5 wherein said emulator device further comprises a Field Programmable Gate Array (FPGA) device.

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

16. In regards to Claim 7,

> 7. A method for performing a stall operation in a system that includes a device under test and an emulator device, said method comprising:
>
> a) executing instructions on said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

> b) emulating the functions of said device under test by operating said emulator device in lock-step fashion with said device under test; and

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> c) performing a stall operation, comprising:
>
>> c1) said device under test conveying clock signals to said emulator device;
>>
>> c2) upon receiving a first signal that indicates that a stall function is to be performed, initiating said stall function at said device under test;
>>
>> c3) upon receiving said first signal, discontinuing said sending of said clock signals from said device under test to said emulator device; and
>>
>> c4) discontinuing execution of said instructions that are performed in lock-step at said emulator device while said sending of said clock signals is discontinued.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

17. In regards to Claim 8,

> 8. The method according to claim 7 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA), said clock signals further comprising signals from said microcontroller central processing unit clock.

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

18. In regards to Claim 9,

> 9. The method of Claim 8 further comprising: resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device under test, said emulator device operable upon receiving said clock signals to resume execution of said instructions that are performed in lock-step.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

19. In regards to Claim 10,

> 10. A method for performing a sleep operation, comprising:
>
>> executing a sequence of instructions by a device under test, said device under test including at least one clock for generating clock signals;
>>
>> executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> receiving a first signal at a register of said device under test that indicates that a sleep function is to be initiated;

> initiating said sleep function at said device under test upon receipt of said first signal;

> turning off said at least one clock of said device under test; and

> discontinuing execution of instructions that are performed in lock-step by

> said emulator device upon said turning off of said clock.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

20. In regards to Claim 11,

> 11. The method according to claim 10 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

21. In regards to Claim 12,

12. The method of Claim 11 wherein said at least one clock includes a microcontroller CPU clock.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

22. In regards to Claim 13,

13. The method of Claim 12 further comprising:

when said sleep function has been completed by said device under test, resuming generation of clock signals at said device under test and coupling said clock signals to said emulator device;

when said sleep function has been completed by said device under test, sending a second signal from said device under test to said emulator device;

receiving said second signal at said emulator device;

determining the number of clock signals received at said emulator device since said second signal was received; and

resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

23. In regards to Claim 14,

14. The method according to claim 13 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

24. In regards to Claim 15,

15. The method of Claim 14 wherein said first signal is a first bit, said sleep function initiated upon the receipt of said first bit at a register of said microcontroller.

Examiner finds that the memory (Fig.7, Item 206) corresponds to claimed register. See col.12, lines 4-11 for more details.

25. In regards to Claim 16,

16. A method for performing a stall operation, comprising:

executing a sequence of instructions by a device under test;

executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

said device under test sending clock signals to said emulator device; receiving a first signal at a register of said device under test that indicates that a stall function is to be initiated;

initiating said stall function at said device under test upon receipt of said first signal;

discontinuing said sending of said clock signals from said device under test to said emulator device upon initiation of a stall function at said device under test; and

discontinuing execution of said sequence of instructions at said emulator device while said sending of said clock signals is discontinued.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

26. In regards to Claim 17,

> 17. The method according to claim 16 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

27. In regards to Claim 18,

> 18. The method according to Claim 17 wherein said clock signals further comprise signals from a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

28. In regards to Claim 19,

> 19. The method of Claim 18 further comprising: resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device under test, said emulator device operable upon receiving said clock signals to resume execution of said sequence of instructions.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

29. In regards to Claim 20,

> 20. The method of Claim 19 wherein said sequence of instructions comprises the core processing functions of said microcontroller.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Examiner finds that the RUN/HALT of the target program applies to all processing functions of the target program 22.

30. In regards to Claim 21,

> 21. An in-circuit emulation system comprising:
>
> > a device under test that executes a sequence of instructions, said device under test operable, upon receiving a first signal, to initiate a stall function;
> >
> > an emulator device for emulating the functions of said device under test, said emulator device operable so as to execute said sequence of instructions in lock-step fashion with said device under test, said emulator device configured for receiving clock signals sent by said device under test; and
> >
> > wherein said device under test sends clock signals to said emulator device, said device under test operable, upon receiving said first signal, to discontinue sending said clock signals to said emulator device, and said emulator device operable, upon said discontinuation of said clock signals from said device under test, to discontinue execution of said sequence of instructions.

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

31. In regards to Claim 22,

> 22. The in-circuit emulation system of Claim 21 wherein said device under test is a microcontroller, said microcontroller operable to resume sending said clock signals to

said emulator device when said stall function has been completed by said
microcontroller, said emulator device operable upon receiving said clock signals to
resume execution of said sequence of instructions.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock
synchronization acknowledge circuit, the controller 228 activates the RESET
signal on line 258 which causes the target bus watch circuit 224 to release the
RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that
the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

32. In regards to Claim 23,

> 23. The in-circuit emulation system of Claim 22 wherein said clock signals further
> comprise signals from a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator
(Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the
target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item
212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently
"internal CPU clocks", because the RUN/HALT signals go to these entities.

33. In regards to Claim 24,

> 24. The in-circuit emulation system of Claim 23 wherein said emulator device comprises
> a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of
FPGAs as emulator devices.

34. In regards to Claim 25,

> 25. An in-circuit emulation system comprising;
>
> > a device under test that executes a sequence of instructions, said device under
> > test operable, upon receiving a first signal, to initiate a sleep function at said device under
> > test and to turn off a clock of said device under test; and
> >
> > an emulator device for emulating the functions of said device under test, said
> > emulator device operable so as to execute said sequence of instructions in lock-step
> > fashion with said device under test, said emulator device operable, upon said turning off
> > of said clock to discontinue execution of said sequence of instructions at said emulator
> > device.

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

35. In regards to Claim 26,

> 26. The in-circuit emulation system of Claim 25 wherein said device under test comprises a microcontroller, said device under test operable when said sleep function has been completed by said device under test to turn on said at least one clock and to send a second signal to said emulator device, said emulator device operable upon receiving said second signal to determine the number of clock signals received at said emulator device since said second signal was received and said emulator device operable to resume execution of said sequence of instructions when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

36. In regards to Claim 27,

27. The in-circuit emulation system of Claim 26 wherein 22 device under test is a microcontroller, said at least one clock further comprising a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

37. In regards to Claim 28,

28. The in-circuit emulation system of Claim 27 wherein said emulator device comprises a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

Response to Amendment

Re: Specification

38. Applicant has amended the specification in the amendment filed 2/10/06 in order

to remedy an objection triggered by a minor informality (a typographical error).

Examiner has withdrawn the objection.

Re: Drawings

39. Applicant's new Figure 7 filed 2/10/06 correctly refers to step 705 in a manner

consistent with the detailed description of the application. Examiner accepts the

new drawing.

Re: Claim Rejections - 35 USC § 102

40. The Applicant unpersuasively argues (see pp.14 of the amendment filed 2/10/06) that the Profit reference does not read upon the claimed invention because Profit teaches a system "where part of the target hardware is modeled by the processor emulator, and part ... is modeled by the hardware simulator running on the host computer."

41. The Applicant then argues (see pp.14 of the amendment filed 2/10/06) that "As such, Profit does not disclose a device under test and an emulator device operating in lock-step fashion with the device under test, as claimed."

42. Examiner respectfully disagrees. Because part of the target hardware (the "device under test") is modeled by the processor emulator, and part is modeled by the hardware simulator running on the host computer, the processor emulator operates in lockstep with the portion of the "device under test" running in the software simulator.

43. Therefore, the Profit reference reads upon the invention as claimed.

44. Examiner finds that Applicant's specification reinforces this interpretation. In Applicant's specification (p.4, emphasis added below), the "device under test" is a microcontroller, and this "device under test" is programmed into the FPGA emulator, which operates in lockstep with a "host PC." Page 4 of Applicants specification teaches the following:

SUMMARY OF THE INVENTION

The method and apparatus of the present invention effectively provides in-circuit emulation using an emulation device that operates in lock-step fashion with the device under test. The method and apparatus of the present invention effectively handles sleep and stall operations such that the emulation device and the device under test continue to operate in lock-step after sleep and stall operations have been performed.

A system that includes a device under test and that includes an emulator device is disclosed. The emulator device emulates the functions of the device under test by operating in lock-step fashion with the device under test. **In one embodiment, the emulator device is a Field Programmable Gate Array (FPGA) device and the device under test is a microcontroller. A host PC can be coupled to the emulator device. The FPGA is programmed to operate as a virtual microcontroller, performing a set of instructions that are also performed by the microcontroller in lock-step fashion.** In the present embodiment, only the core processing functions of the microcontroller are performed in lock-step fashion.
However, alternatively, any or all instructions or sequences of instructions performed by the microcontroller could be performed in lock-step fashion by the FPGA.

Conclusion

45. Applicant's arguments filed 10/12/2005 have been fully considered but they are

not persuasive.

Correspondence Information

Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Ayal I. Sharon whose telephone number is

(571) 272-3714. The examiner can normally be reached on Monday through

Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753.

Any response to this office action should be faxed to (703) 872-9306,

or mailed to:

> USPTO
> P.O. Box 1450
> Alexandria, VA 22313-1450

or hand carried to:

> USPTO
> Customer Service Window
> Randolph Building
> 401 Dulany Street
> Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application

or proceeding should be directed to the Tech Center 2100 Receptionist, whose

telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
April 4, 2006

Paul P. Rodriguez   1/7/06

Supervisory Patent Examiner
Art Unit 2152123